

LH532000B

CMOS 2M (256K × 8/128K × 16)
Mask-Programmable ROM

FEATURES

- 262,144 words × 8 bit organization (Byte mode)
131,072 words × 16 bit organization (Word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access times: 120/150 ns (MAX.)
- Low-power consumption:
Operating: 275 mW (MAX.)
Standby: 550 μW (MAX.)
- Programmable $\text{OE}/\overline{\text{OE}}$ and $\text{OE}_1/\overline{\text{OE}}_1/\text{DC}$
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
 - 40-pin, 600-mil DIP
 - 40-pin, 525-mil SOP
 - 48-pin, 12 × 18 mm² TSOP (Type I)
- ×16 word-wide pinout

DESCRIPTION

The LH532000B is a 2M-bit mask-programmable ROM with two programmable memory organizations, byte and word modes. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

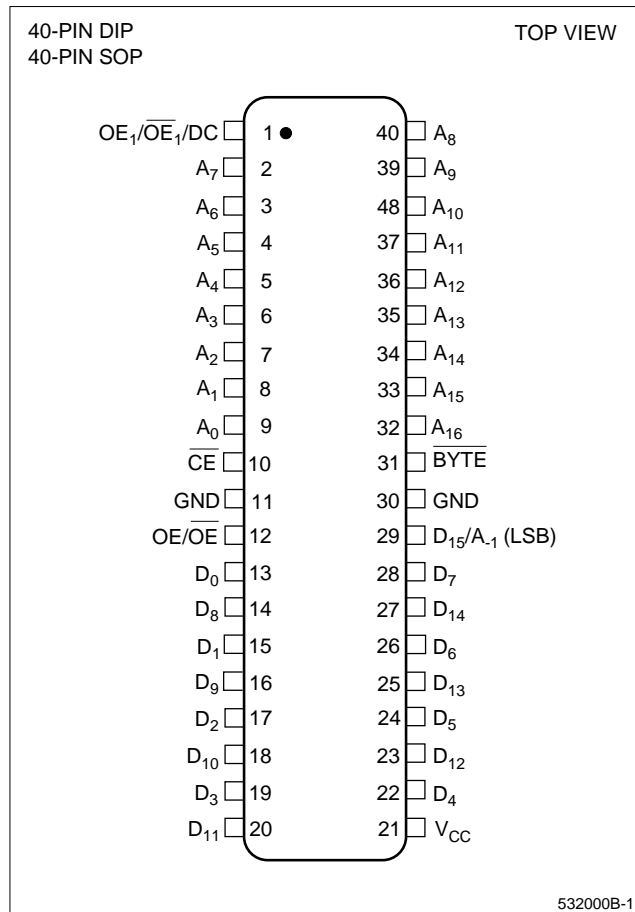


Figure 1. Pin Connections for DIP and SOP Packages

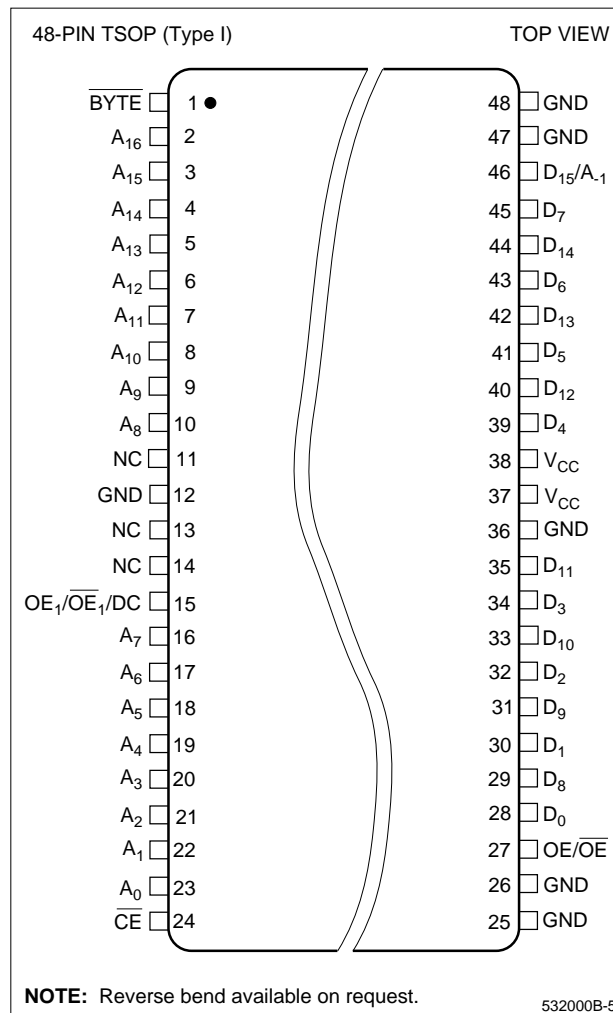


Figure 2. Pin Connections for TSOP Package

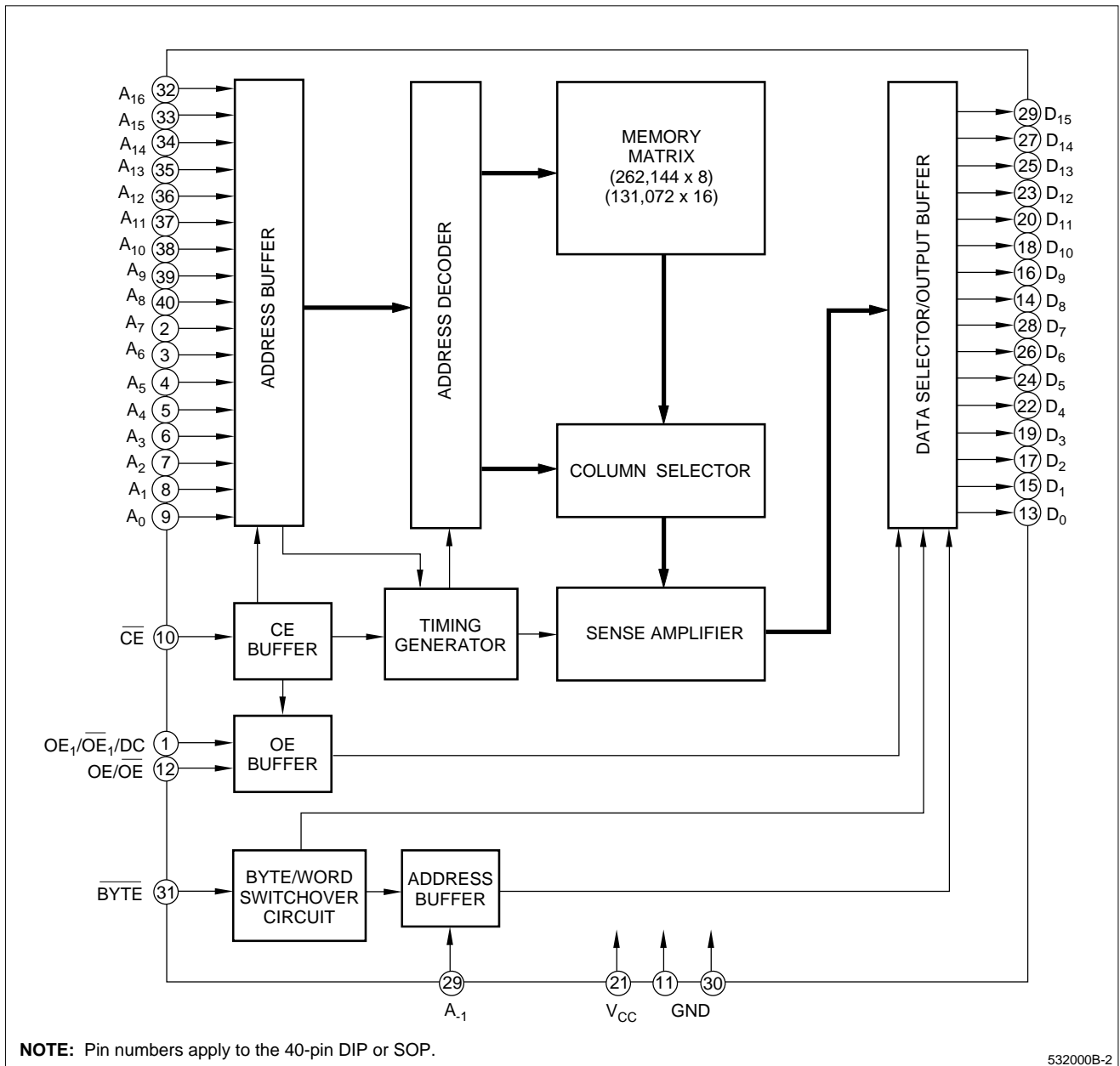


Figure 3. LH532000B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A ₋₁	Address input (BYTE mode)	1
A ₀ – A ₁₆	Address input	
D ₀ – D ₁₅	Data output	1
\overline{CE}	Chip enable input	
OE/OE	Output enable input	2

SIGNAL	PIN NAME	NOTE
OE ₁ / \overline{OE} ₁ /DC	Output enable input or Don't care	2
\overline{BYTE}	Byte/word mode switch	
V _{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

1. D₁₅/A₋₁ pin becomes LSB address input (A₋₁) when the bit configuration is set in byte mode, and data output (D₁₅) when in word mode. BYTE input pin selects bit configuration.
2. The active levels of OE/OE and OE₁/ \overline{OE} ₁/DC are mask-programmable. Selecting DC allows the outputs to be active for both high and low levels applied to this pin. It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

\overline{CE}	OE/ \overline{OE}	OE ₁ / \overline{OE} ₁	\overline{BYTE}	A ₋₁ (D ₁₅)	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
					D ₀ – D ₇	D ₈ – D ₁₅	LSB	MSB	
H	X	X	X	X	High-Z	High-Z	–	–	Standby (I _{SB})
L	L/H	X	X	X	High-Z	High-Z	–	–	Operating (I _{CC})
L	X	L/H	X	X	High-Z	High-Z	–	–	Operating (I _{CC})
L	H/L	H/L	H	Input inhibit	D ₀ – D ₇	D ₈ – D ₁₅	A ₀	A ₁₆	Operating (I _{CC})
L	H/L	H/L	L	L	D ₀ – D ₇	High-Z	A ₋₁	A ₁₆	Operating (I _{CC})
L	H/L	H/L	L	H	D ₈ – D ₁₅	High-Z	A ₋₁	A ₁₆	Operating (I _{CC})

NOTE:

1. X = H or L, High-Z = High-impedance.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V _{CC}	–0.3 to +7.0	V
Input voltage	V _{IN}	–0.3 to V _{CC} + 0.3	V
Output voltage	V _{OUT}	–0.3 to V _{CC} + 0.3	V
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V _{IL}		–0.3		0.8	V	
Input 'High' voltage	V _{IH}		2.2		V _{CC} + 0.3	V	
Output 'Low' voltage	V _{OL}	I _{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V _{OH}	I _{OH} = –400 μA	2.4			V	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}			10	μA	
Output leakage current	I _{LO}	V _{OUT} = 0 V to V _{CC}			10	μA	1
Operating current	I _{CC1}	t _{RC} = t _{RC} (MIN.)			50	mA	2
	I _{CC2}	t _{RC} = 1 μs			45		
	I _{CC3}	t _{RC} = t _{RC} (MIN.)			45	mA	3
	I _{CC4}	t _{RC} = 1 μs			40		
Standby current	I _{SB1}	$\overline{CE} = V_{IH}$			3	mA	
	I _{SB2}	$\overline{CE} = V_{CC} - 0.2 V$			100		
Input capacitance	C _{IN}	f = 1 MHz			10	pF	
Output capacitance	C _{OUT}	T _A = 25°C			10		

NOTES:

- OE/ \overline{OE} ₁ = V_{IL}, $\overline{CE}/\overline{OE}/\overline{OE}$ ₁ = V_{IH}
- V_{IN} = V_{IH} or V_{IL}, $\overline{CE} = V_{IL}$, outputs open
- V_{IN} = (V_{CC} – 0.2 V) or 0.2 V, $\overline{CE} = 0.2 V$, outputs open

AC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0\text{ to }+70^\circ\text{C}$)

PARAMETER	SYMBOL	120 ns		150 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	120		150		ns	
Address access time	t_{AA}		120		150	ns	
Chip enable access time	t_{ACE}		120		150	ns	
Output enable delay time	t_{OE}		55		70	ns	
Output hold time	t_{OH}	5		10		ns	
CE to output in High-Z	t_{CHZ}		55		70	ns	1
OE to output in High-Z	t_{OHZ}		55		70	ns	

NOTE:

1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

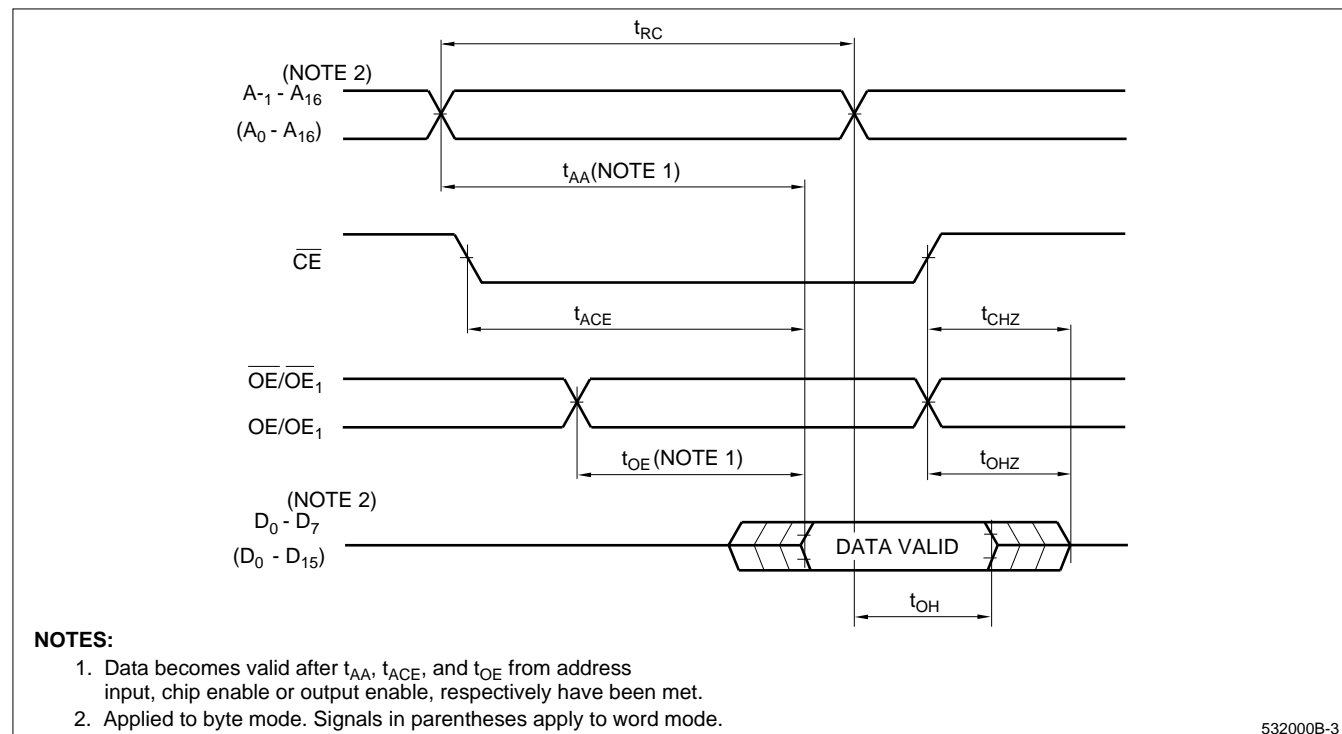
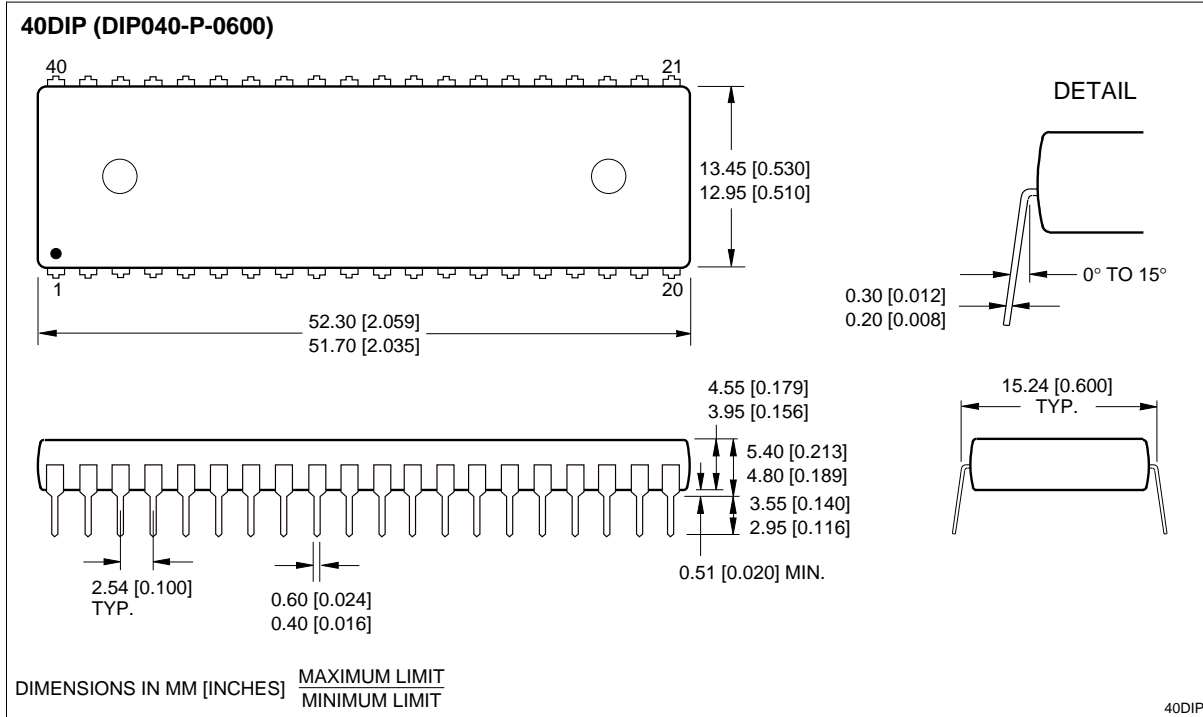
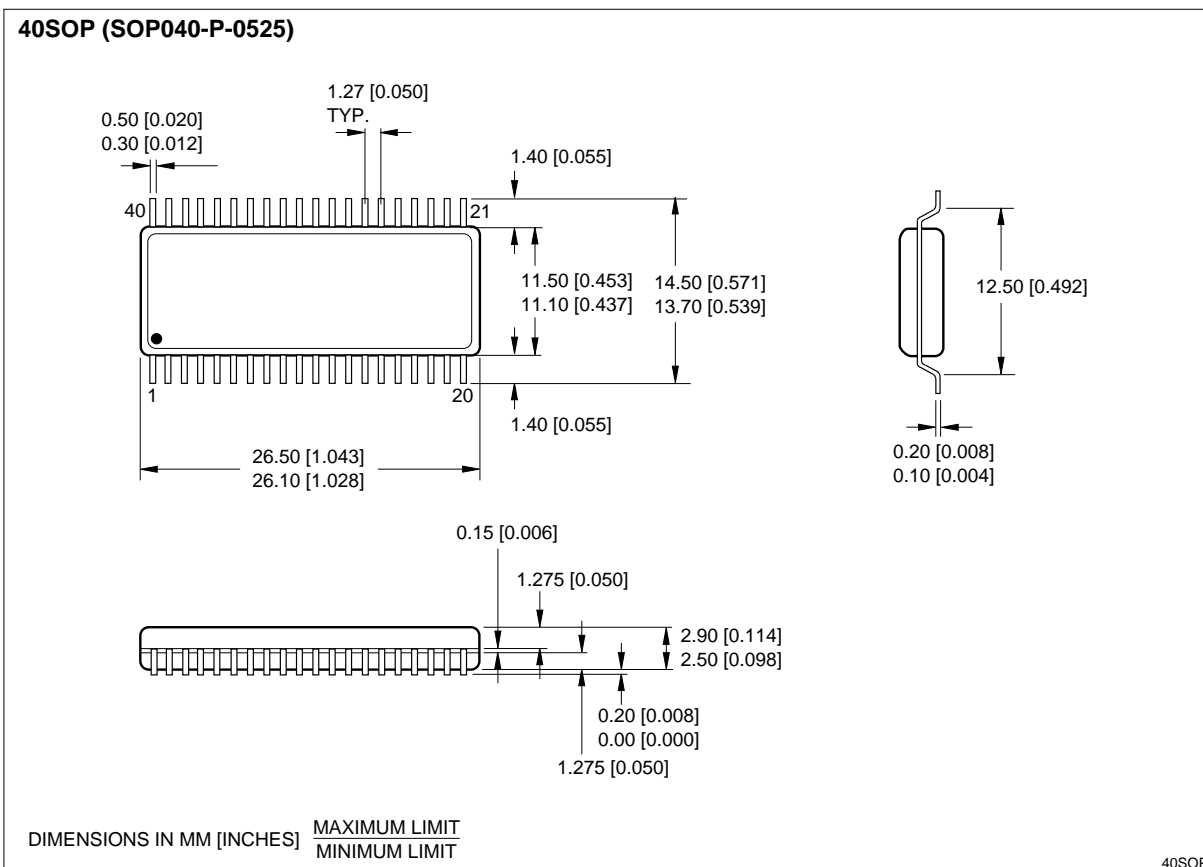


Figure 4. Timing Diagram

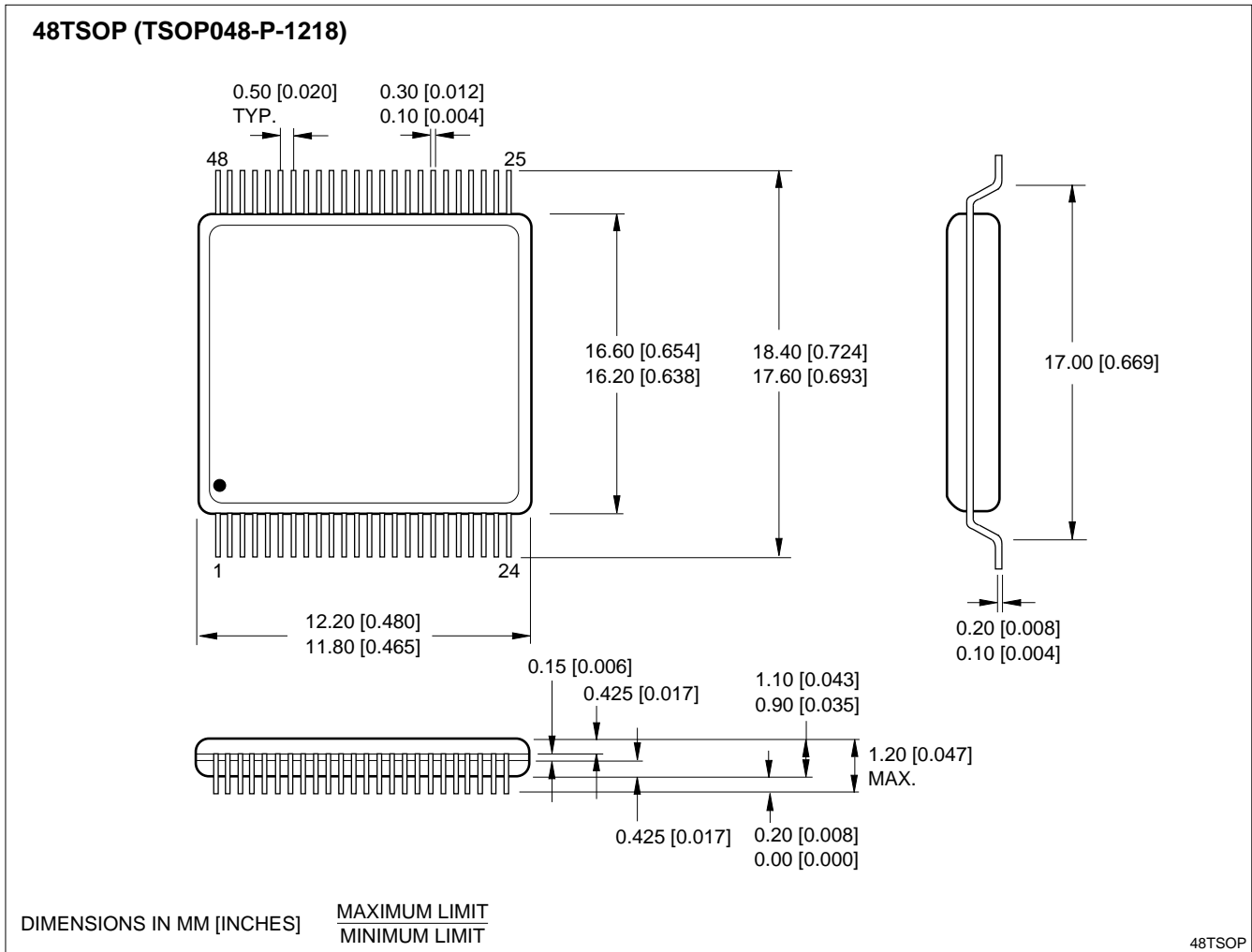
PACKAGE DIAGRAMS



40-pin, 600-mil DIP

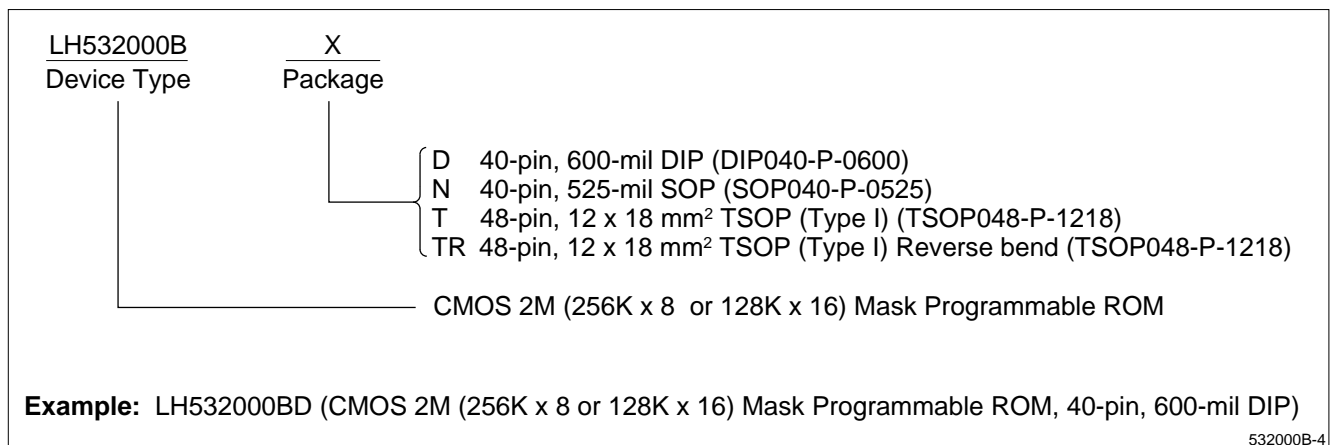


40-pin, 525-mil SOP



48-pin, 12 × 18 mm² TSOP (Type I)

ORDERING INFORMATION



532000B-4